Negative gate capacitance devices

The subthreshold slope and overall performance of the device are reportedly improved in a DMG TFET. 28 Taking stock of these features, ... of four distinct structures, namely (1) C-SMTFET (single metal gate-negative capacitance-tunnel field-effect transistor), (2) C-DMTFET (dual metal gate-negative capacitance-tunnel field-effect ...

The reduction in the power consumption of large-scale devices is expected to cause a surge in demand for FET technology in the near future. Negative-capacitance FETs (NC-FETs) with ferroelectric ...

Analytical models are presented for a negative capacitance double-gate tunnel field-effect transistor (NC DG TFET) with a ferroelectric gate dielectric in this paper. The model accurately calculates the channel potential profile by solving the Poisson equation with the Landau-Khalatnikov (LK) equation. Moreover, the effects of the channel mobile charges on the ...

The unique feature which makes these devices suitable for ultra-low voltage operation is the steep slope achieved by negative capacitance of the ferroelectric oxide based gate stack.

Here we report the ZrOx-based negative capacitance (NC) FETs with 45.06 mV/decade subthreshold swing (SS) under ± 1 V VGS range, which can achieve new opportunities in future voltage-scalable NCFET applications. The ferroelectric-like behavior of the Ge/ZrOx/TaN capacitors is proposed to be originated from the oxygen vacancy dipoles. The NC effect of the ...

This so-called Boltzmann Tyranny is mainly dependent upon two factors: (1) body factor and (2) transport factor. This issue is mitigated either by optimizing the transport factor or body factor [14], [15].To push the limit of body factor, the devices like Micro-Electro-Mechanical-Systems (MEMS) based FET or Suspended-Gate (SG) MOSFET (SG-MOSFET), ...

In this paper, approaches to obtain the sub-kT/q non-hysteretic operation mode in negative capacitance (NC) FETs for a wide band of applied gate voltages, using capacitance matching, were ...

The NC concept has drawn much attention for promising to provide room temperature sub-60 mV/decade subthreshold swing in FET devices. The original idea was proposed by Salahuddin and Datta in 2008 [8] supporting that the Landau-Devonshire theory would lead to an intrinsic NC region in a ferroelectric capacitor. This region could be effectively ...

current CMOS fabrication method. The transistor''s gate stack of an NCFET contains a ferroelectric (FE) layer that exhibits a negative capacitance effect that amplifies the internal voltage. However, it remains a challenging task to realize the stable negative capacitance in the non-hysteretic non-transient regime.

The ferroelectric negative capacitance (NC) draws a great deal of attention for low-power negative

capacitance field-effect transistors (NCFET) and NC capacitors. The fabrication of steep-slope FET (subthreshold swing < 60mVdec -1) is reported, followed by modeling approaches. While the device fabrication favors a ferroelectric gate structure ...

a, Energy landscape U of a ferroelectric capacitor in the absence of an applied voltage. The capacitance C is negative only in the barrier region around charge Q F = 0. b,c, Evolution of the ...

Negative Capacitance Fin field-effect transistor (NC-FinFET), due to its superior gate electrostatics and dominance over the short channel effects (SCEs), has been the key technology over the ...

Superior gate electrostatics and dominating control over short-channel effects (SCEs) set the Negative Capacitance Fin Field-Effect Transistor (NC-FinFET) apart from conventional devices. However, advancements in device performance through various engineering strategies have prompted further progress in NC-FinFET technology. This work ...

Integrating ferroelectric negative capacitance (NC) into the field-effect transistor (FET) promises to break fundamental limits of power dissipation known as Boltzmann tyranny.

In this study, we have found a solution to suppress the negative gate capacitance for $text{CSTBT}^{text{TM}}$, enabling the reduction in $mathrm{V}_{text{CEsat}}$ by using a split-gate structure. Additionally, we have clarified the mechanism through a combination of measurements and device simulations. As a result, the ...

The gate capacitance of MOS-gated power devices during the on state is analyzed by experimental measurements and simulations. Negative gate capacitances are found during turn-on transients and ...

The total gate capacitance C total is plotted as function of external gate voltage V GNC for three different materials. The peak obtained in the graph corresponds to the Negative Capacitance region. HfSiO shows the highest peak value of 6.2 µF/cm 2 because of the better capacitance matching in comparison to other materials as evident from the ...

A negative capacitance transistor has this property that the gate stack contributes to the differential voltage amplification and enhances the surface potential at a given gate voltage from weak ...

The paper discusses the development of various negative capacitance field-effect transistors from their initial stages until recent modifications. The incorporation of ...

Here, we experimentally demonstrate the steep switching behavior of a MOS device-i.e., SS ~ 18 mV/decade (much less than 60 mV/decade) at 300 K-by taking advantage of negative capacitance in a MOS ...

Due to the widespread usage of 1.2kV IGBTs for low and medium voltage applications, for the first time, this

paper investigates the influence of technology on the instability effect of negative gate capacitance (NGC) in IGBT technologies - NPT (non punch-through), PT (punch-through) and FS (field stop). Due to the high density of plasma during forward ...

Negative capacitance in ferroelectric materials was proposed in 2008 by Salahuddin and Datta to provide voltage amplification without needing to design a totally new ...

This article shows that the dynamic avalanche and the negative gate capacitance can be suppressed by the management of the electric field concentration and ...

where, a, v, g are material parameters, E is the external applied electric field, and P is the polarization of the ferroelectric. For a negative capacitor, a is always negative [].Although the Landau theory allows for a phenomenological interpretation of ferroelectric behavior (based on a mean-field approach []), it can be shown that the Gibb"s free energy as ...

A simulation-based analysis of negative capacitance double-gate junctionless transistor (NCDGJLT) is presented in this paper. The effect of variation in the thickness of ferroelectric material (t f), gate oxide (t ox), and silicon channel (t Si) on electrical characteristics of device is analyzed is found that NCDGJLT can reduce OFF state current, ...

In contrast to the recent report 6 showing a negative capacitance effect in a 2D device with relatively high gate voltages (close to -10 V) and hysteretic features in a structure with a metal ...

through self-consistent device and circuit models that are calibrated to experimental mea-surements. First, the 101-stage ring oscillator consisting of 14 nm FinFET devices with a ferroelectric gate layer that exhibits negative capacitance are used to study the response speed of the negative capacitance effect.

By using a negative-capacitance gate stack, the supply voltage (V dd) applied to the gate of the CFET is increased, resulting in a reduction in power consumption. Here, we ...

This article presents a study on the subthreshold swing (SS) and the ON-OFF current ratio of a negative capacitance source pocket double-gate tunnel field-effect transistor (NC-SP-DGTFET). In this analysis, a novel device is developed that integrates gate and channel engineering techniques. The combination of the ferroelectric material hafnium zirconium oxide ...

The novel device structure of negative capacitance gate all around field effect transistor (NC GAA-FET) can combine both the advantages of GAA-FET and NC-FET, and is the most ...

Boltzmann electron energy distribution poses a fundamental limit to lowering the energy dissipation of conventional MOS devices, a minimum increase of the gate voltage, i.e. 60 mV, is required for ...

Negative gate capacitance devices

Is there any device that unambiguously demonstrated negative capacitance? The answer is yes. The negative capacitance associated with a micro-electro-mechanical (MEM) switch can be unambiguously stabilized at ...

Apart from these, an alternate way to reduce the device SS can be achieved by modifying the capacitance matching of channel capacitance and gate dielectric layer capacitance. This kind of device includes junctionless nanowire transistors [19] and ultra-thin bulk silicon SOI transistors [20]. However, it is noteworthy to remember that these ...

With a suitable design, a negative capacitance field-effect transistor (NC-FET) should, in principle, achieve a subthreshold swing below the 60 mV per decade thermionic ...