Capacitor Calibration

area for auxiliary calibration capacitors. Introduction: It is well known that SAR ADCs have nonlinearities due to capacitor mismatch, which makes it difficult to improve the accuracy. In order to improve the SNDR (Signal-to-Noise and Distortion Ratio) of SAR ADCs, many design methods for capacitor calibration have been proposed in the industry.

The conversion accuracy of successive approximation register (SAR) analog-to-digital converter (ADC) is mainly affected by the capacitor mismatch. In this brief, a ...

calibration capacitor. 5371A10. Capacitance: 0.011 nF Voltage: 30 V... o High insulation (10E14 O) This is a high precision capacitor with excellent insulation. In combination with a precise voltage source, charge signals may be generated as needed. The capacitor Type ...

In this paper, a novel capacitor self-calibration technique is presented, which can be used in high resolution ADCs, such as SAR ADC and pipeline ADC. The capacitors achieve self-calibration through the adjusting capacitors array and successive approximation (SAR) logic. A 14-bit SAR ADC using capacitor self-calibration technique we proposed has been designed. ...

A 16-bit 1-MS/s SAR ADC was fabricated in 180nm digital CMOS. To maintain excellent linearity, a window capacitor calibration (WCC) scheme is proposed to estimate capacitor mismatch and obtain corrected bit weights. Different from prior calibration schemes, the WCC scheme can alleviate the offset and flicker noise effects on the calibration accuracy. The total input ...

The Teseq INA 3601 Surge Calibration Capacitor is a high-quality and reliable instrument used for surge testing and calibration purposes. Manufactured by Schaffner, a renowned company in the field of EMC testing equipment, this capacitor is ...

Remaining within 0.1% of original calibration, the kit is a close-tolerance, stable capacitor set with calibration traceable to the National Bureau of Standards. Use of four capacitors plus the adapter makes any capacitance value accurate to four significant figures with ±0.1% tolerance.

The excellent precision of repetitive substitution procedures is exploited by step-up or step-down methods to extend measurements to higher or lower magnitudes without serious degradation ...

This paper presents a capacitor calibration technique called median selection for improving the static and dynamic performance of the successive approximation register (SAR) analog-to-digital converter (ADC). Monte Carlo simulations in MATLAB are presented to demonstrate the effect of the proposed method. Simulation results show that for an 18-bit RC ...

A foreground digital self-calibration technique has been described. The calibration technique improves

capacitor matching without using additional circuits and extensive computation. Applied to a 12 bit SAR ADC with 10% capacitor mismatch, SNDR is increased from 44.12 to 72.85 dB, resulting in 4.77 bit improvement of ENOB.

The ADC adopts a mixed digital-analog design scheme, in which the internal comparator, latch, DAC capacitor array, etc., are analog parts, and the rest of the SAR algorithms and calibration algorithms are all implemented in digital Verilog code, with a conversion accuracy of 0.8 mV and a calibration accuracy of 0.5 LSB.

This paper presents a high-resolution 18-bit SAR ADC with a high 10-bit capacitor DAC and a low 8-bit resistor DAC. The total required number of the unit capacitors is decreased to 512. Foreground digital calibration based on capacitive recombination is introduced to improve linearity. Preamplifiers and output offset storage(OOS) enhance the noise and offset ...

Accurate calibration of capacitors that range in value from 0.01 mF to 100 mF over the frequency range from 100 Hz to 100 kHz is desired. There are several instruments available commercially to measure the impedance of a capacitor.

Capacitance Calibration. The precision measurement of capacitors for the purpose of calibration is generally based on a national primary standard of high accuracy, secondary/working ...

factor from the calibration reference standard capacitors to the customer fused-silica standard capacitors. The procedure is similar for other types of 3T standard capacitors (air/nitrogen-dielectric, ceramic), although the uncertainty changes slightly, dependent upon the relative quality of the capacitor.

The proposed C-R DAC consists of an 8-bit CDAC, a 2-bit RDAC, and a calibration capacitor. Each capacitor of the upper 5-bit capacitors is determined by the sum of C N and C N ". The calibration capacitor is composed of a minimum unit of 0.25C, so the capacitor calibration of the C-R DAC is performed with a resolution of 1/4 LSB.

The capacitance mismatch problem limits the accuracy improvement of high-precision SAR ADCs (Successive Approximation Register Analog-to-Digital Converters). To address the capacitance array mismatch in SAR ADCs, this paper proposes a novel capacitor calibration scheme based on the Time-to-Digital Converter (TDC). This scheme achieves ...

In Fig. 1, during the foreground calibration phase, the capacitor recombination digital module receives the output of the comparator during the capacitors comparison and obtains the sorting results of capacitors size.During the normal conversion phase, the SAR logic control module controls the optimal capacitor after capacitor recombination by controlling ...

With 50+ years of stability data and history, IET Labs manufactures a full line of standard capacitors that will

cover most any budget and application. ... IET Labs, maintains some of the finest R, L and C calibration standards in the World. IET"s capacitance standards are manufactured with pride in the USA. SCA Series Capacitance Standard .

Capacitance Calibration - Capacitance Standards and Service . IET Labs is a premier calibration laboratory that is accredited by A2LA for Capacitance-Measure and Capacitance-Generate.. We can calibrate most capacitance standards or capacitance decades from 10 aF - 10 F with some of the best measurement uncertainties, as good as 4.8 µF/F, of any commercial ...

errors, the capacitors in the DAC of a SAR ADC suffer from mi smatch, thus limiting the converter"s resolution. To improve matching, large capacitors are used, but at the expense of reduced speed and increased power consumption and area [1, 2]. An alternative approach is to use calibration to trim capacitors to reduce the mismatch [3, 4],

A foreground digital self-calibration technique has been described. The calibration technique improves capacitor matching without using additional circuits and extensive computation. Applied to a 12 bit SAR ADC ...

The service for high-voltage capacitors provides measurements of capacitance and dissipation factor at applied voltages ranging from. 100 V to 170 kV at 60 Hz depending on the nominal ...

IET is the World"s Leading Capacitance Standard Manufacturer. With 50+ years of stability data and history, IET Labs manufactures a full line of standard capacitors that will cover most any ...

This document describes the capacitance calibration service provided by NIST, including measurement procedures and systems used to calibrate capacitance standar ... Also included are summaries of calibration uncertainties of capacitors of various dielectric materials, such as fused-silica, nitrogen, air, and mica. Citation. Special Publication ...

These high precision calibration capacitors come with excellent insulation. In combination with a precise voltage source, charge signals may be generated as needed. The family Type 5371A is ideally suited to verify the functionality of charge amplifiers and to simulate the output signal of a piezoelectric sensor for development purposes.

What types of precision capacitors and calibration capacitors does Electrocube offer? Electrocube"s wide selection of film capacitor manufacturing and precision capacitor sales includes: Audio-optimized Film Capacitors; Custom Film Capacitors; High Temperature Film Capacitors; pfc Precision Film Capacitors and Standards; Standard Film Capacitors

To address the capacitance array mismatch in SAR ADCs, this paper proposes a novel capacitor calibration scheme based on the Time-to-Digital Converter (TDC). This scheme achieves calibration accuracy as high as

0.01% and can be flexibly designed to meet the accuracy requirements of SAR ADCs. Simulation results indicate that the capacitance ...

The capacitor reconstitution calibration method is introduced with the example of a 14-bit hybrid capacitive-resistive SAR ADC with a high M-bit capacitive DAC and a low N-bit resistive DAC, as shown in Fig. 1. If M = 8 and N = 6, it represents a 14-bit SAR ADC consisting of a high 8-bit capacitive DAC and a low 6-bit resistive DAC. In the ...

Accurate calibration of capacitors that range in value from 0.01 mF to 100 mF over the frequency range from 100 Hz to 100 kHz is desired. There are several instruments available commercially ...

HFXO Capacitor Bank (CTune) calibration on EFR32 Content. What is CTune; How to configure CTune; Preventing real-time configuration; Measurements, calibration of CTune; The following KBA was written using an EFR32MG14 radio board (BRD4169A) under Flex SDK 2.5.1 (RAIL 2.6), but the process should be the same on all EFRs and all Flex SDKs ...

A radix of 1.85 is chosen in our design, resulting in 14 conversion steps to achieve 12 bits. The capacitor array utilizes customized metal-oxide-metal (MOM) capacitors with a minimum capacitance value of ...

This brief presents a 16-bit successive approximation register (SAR) analog-to-digital converter (ADC) with input- signal-independent background calibration. A serial double conversion (SDC) method with second MSB decisions skipped is proposed to perform A/D conversion and background calibration simultaneously, with only one ADC and little extra ...

This document describes the capacitance calibration service provided by NIST, including measurement procedures and systems used to calibrate capacitance standards of ...

This paper presents a fully differential 12-bit SAR ADC with a novel capacitor mismatch calibration. The calibration calculates the capacitor mismatch via the metastability of the comparator and statistical method. A novel metastability detection circuit is designed to ensure the detection accuracy and avoid the "fake metastability" problem. Post-simulation shows that the ...

According to the thermometer codes, DWA logic operates to control the sampling capacitors to generate the residue of the first stage. Then, the residue is magnified times by the inter-stage amplifier and sampled by the second stage. At the same time, the most significant bit (MSB) capacitor of the second stage,, is connected to positive reference or negative ...

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