Based on the calibration mechanism of capacitors

This brief presents a simple capacitor mismatch calibration in SAR ADCs, which is in foreground and on chip. Capacitor errors are extracted based on output histogram under a triangular input signal generated on chip and compensated by tuning capacitors with a calibration DAC. A novel one-by-one strategy can simplify the ...

Energy storing and dissemination of the electrolyte ions to the electrode surface area is the basis operation principle of supercapacitors. Supercapacitors are ...

An all-digital, histogram-based calibration technique to correct capacitor mismatch in successive-approximation register (SAR) ADCs is proposed, using a windowing technique to detect non-uniform code densities and recursively tunes the bit weights toCorrect capacitor errors. An all-digital, histogram-based calibration ...

A novel dithering-based calibration technique to correct capacitor mismatch in digital-to-analogue converter (DAC) used in successive approximation register analogue-to-digital converters is proposed...

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The asymmetric capacitor is set up with carbon-based electrode as a negative electrode and metal oxides as a positive electrode [33]. Asymmetric hybrid capacitors that connect these two electrodes reduce the effects of this conflict, permitting them to attain better energy and power densities than conventional EDLCs.

Variable Capacitors: Look for a mechanism for adjusting capacitance, such as a screw or knob. Variable capacitors often have a larger size compared to other types, with visible plates and a movable rotor. They may be labeled with capacitance values or tuning ranges. Trimmer Capacitors:

The mechanism and theoretical approach we report is general and can be used to computationally screen new materials for improved pseudocapacitive charge storage.

2 =0, the normal conversion continues and no calibration operation happens. Proposed dithering-based calibration: As illustrated in Fig. 1, the proposed calibration does not require additional analogue circuits. Assuming capacitors in the MSB section suffer from mismatches and the LSB capacitors are ideal, the weights of the MSB and LSB sections

are mainly divided into foreground calibration and background calibration. The DAC capacitor mismatch calibration is mainly performed by the LMS-based background calibration[7,11-14,17,20].Aperturbation-injectedleast-mean-square-based(LMS-based) calibration algorithm

is presented to calibrate DAC capacitor mismatch but at

a capacitor based on MOSFET to achieve constant capaci-tance. Reference 22 proposed a capacitor composed of two PMOS-based channel-gate capacitors in series. The changes of two pre-biased sub-capacitors compensate each other to guarantee the total capacitor constant. However, it requires dedicated clock ...

This paper proposes a new digital enhanced V2-type constant on-time control architecture for solving the ripple oscillation issues when using low-equivalent series resistance (ESR) capacitors in a buck converter. Instead of directly sensing the inductor current, an inductor current ramp estimator with the drift compensation is presented as ...

The calibration is very important to improve the accuracy of the parallel mechanism. This paper proposed a new calibration approach for the parallel mechanism based on the direct kinematics model and the genetic algorithm. The proposed calibration approach avoids the measurement of the absolute position/posture of the moving ...

A digital background calibration technique for pipelined successive approximation register (SAR) analogue-to-digital converters (ADCs) with detect-and-switching (DAS) algorithm is proposed, which reduces the amplitude of the injected dithering signal by only injecting the capacitor mismatch into first-stage residue voltage.

A calibration matrix T transforms the capacitance variation values into the six-dimensional force. Furthermore, the normalized calibration matrix can be obtained by applying individually the rated magnitudes for the six force components. 2.3. Design of the 3D capacitor for six-axis force sensor

Accurate calibration of capacitors that range in value from 0.01 mF to 100 mF over the frequency range from 100 Hz to 100 kHz is desired. There are several instruments ...

This calibration technique does not require any extra capacitor DAC and is programmable for any radix-3 SAR ADC. 7 bit Radix-3 ADC is designed which can achieve signal to noise and distortion ...

Metalized film capacitor degradation under ultra-high electric fields is crucial for the reliability of VSC-HVDC systems. In the present study, systematic investigations were performed that ...

The statistical analysis of the standard deviation of INL and DNL versus different unit capacitance C 0 are analyzed (s I N L $sigma _{INL}$ and s D N L $sigma _{DNL}$) based on 1000 times Monte Carlo runs.The unit capacitor is modeled as a gaussian random variable with mean of C 0 and standard deviation of s 0 [].Moreover, ...

A novel dithering-based calibration technique to correct capacitor mismatch in digital-to-analogue converter

(DAC) used in successive approximation register analogue-to-digital converters is proposed.

Supercapacitors are categorized based on the charge storage mechanisms: one is EDLC which uses the high surface area with tunable porous ...

The unique charge storage mechanism of hydrous ruthenium oxide (Fig. 7 (c)) means that it behaves primarily as a double layer capacitor at all scan rates, with C D contributions only reaching ~25% at the lowest scan rate. Download: Download high-res image (519KB) Download: Download full-size image; Fig. 7.

Classification of electrochemical capacitors based on charge storage mechanism: EDLCs, Pseudocapacitors (Intrinsic and extrinsic). The concept of electrochemical SCs comes from the existence of the EDL present at the interface between a conductor and its electrolyte. The EDL theory is the basis of electrochemical charge ...

Histogram-based calibration of capacitor mismatch in SAR ADCs Eric Swindlehurst and Shiuh-hua Wood Chiang An all-digital, histogram-based calibration technique to correct capaci-tormismatchinsuccessive-approximationregister(SAR)ADCsispro-posed. Using a windowing technique to detect non-uniform code

An all-digital, histogram-based calibration technique to correct capacitor mismatch in successive-approximation register (SAR) ADCs is proposed. Using a windowing technique to detect non-uniform code densities, the calibration recursively tunes the bit weights to correct capacitor errors.

Historical overview of electrochemical capacitors and origin of pseudocapacitors. The charge storage mechanisms of electrochemical SCs are characterized as follows and shown in Fig. 1:(i) electric double layer (EDL) charge storage mechanism, also known as the non-faradaic charge storage mechanism. No charge ...

There is an important distinction between the calibration of voltage transformers and capacitors at NIST. The voltage transformer calibration is of the direct null type, and ...

The features of the wide band gap SiC semiconductor use in the capacitive MOSFE sensors" structure in terms of the hydrogen gas sensitivity effect, the response speed, and the measuring signals" optimal parameters are studied. Sensors in a high-temperature ceramic housing with the Me/Ta2O5/SiCn+/4H-SiC structures and two types ...

This paper presents a high-resolution 18-bit SAR ADC with a high 10-bit capacitor DAC and a low 8-bit resistor DAC. The total required number of the unit capacitors is decreased to 512. Foreground digital calibration based on capacitive recombination is introduced to improve linearity. Preamplifiers and output offset ...

A good linear relationship between ln (J) and E 1 / 2 can be obtained in the low and high electric field regions

for all three types of capacitors. Based on the slopes of the fitted straight lines in the low electric field region, e low are extracted as 9.65, 9.42, and 9.67, respectively, which are very close to the relative permittivity of Al ...

A novel dithering-based calibration technique to correct capacitor mismatch in digital-to-analogue converter (DAC) used in successive approximation register analogue-to-digital converters is proposed. With dithering, weights of most significant bit capacitors can be measured accurately, which relaxes matching requirement in ...

Capacitance Calibration. The precision measurement of capacitors for the purpose of calibration is generally based on a national primary standard of high accuracy, ...